WHAT IS CLAIMED IS:

1. A plate-line over-driven access method for ferroelectric memory comprising the steps of:

raising the voltage in a plate line of the ferroelectric memory to generate a voltage difference between a positive and a negative bit lines of the ferroelectric memory;

providing a first leakage current and a second leakage current to the positive bit line and the negative bit line respectively to enlarge the voltage difference;

enabling a sense amplifier of the ferroelectric memory to further enlarge the voltage difference; and

sensing the voltage difference between the positive and the negative bit lines and outputting the contents stored at the ferroelectric memory accordingly.

2. The plate-line over-driven access method according to claim 1, wherein the sense amplifier is a latch sense amplifier and when the latch sense amplifier is enabled, the higher voltage among the voltage in the

positive bit line and the voltage in the negative bit line is raised to high level whereas the lower voltage is reduced to low level.

3. A bit-line over-driven access method for ferroelectric memory comprising the steps of:

pre-charging a positive bit line and a negative bit line of the ferroelectric memory to raise the voltages in the positive and the negative bit lines to high levels;

enabling a word line of the ferroelectric memory to generate a voltage difference between the positive and the negative bit lines;

providing a first leakage current and a second leakage current to the positive bit line and the negative bit line respectively to further enlarge the voltage difference;

enabling a sense amplifier of the ferroelectric memory; and

sensing the voltage difference between the positive bit line and the negative bit line and outputting the content stored at the ferroelectric memory accordingly.

4. The bit-line over-driven access method according to claim 3, wherein

the sense amplifier is a latch sense amplifier and when the latch sense amplifier is enabled, the higher voltage among the voltage in the positive bit line and the voltage in the negative bit line is raised to high level while the lower voltage is reduced to low level.

5. A ferroelectric memory comprising:

a sense amplifier; and

a memory unit, coupled to the sense amplifier, comprising:

a positive bit line and a negative bit line which are parallel to each other and are coupled to the sense amplifier;

a word line which is virtually perpendicular to the positive and the negative bit lines;

a positive memory cell which is coupled to the word line and will be connected to the positive bit line when the word line is enabled;

a negative memory cell which is coupled to the word line and will be connected to the negative bit line when the word line is enabled;

a plate line which is coupled to the positive and the negative

memory units;

a first current source which is coupled to the positive bit line; and

a second current source which is coupled to the negative bit line.

6. The ferroelectric memory according to claim 5, wherein the ferroelectric memory is applied in a plate-line driven access method, of which, the first current source flows to ground from the positive bit line while the second current source flows to ground from the negative bit line.

7. The ferroelectric memory according to claim 6, wherein the first current source and the second current source, which individually comprise an N-type transistor, are conducted according to an over-driven signal.

8. The ferroelectric memory according to claim 5, wherein the ferroelectric memory is applied in a bit-line driven access method, of which, the first current source flows to the positive bit line while the second current source flows to the negative bit line.

9. The ferroelectric memory according to claim 8, wherein the first current source and the second current source, which individually comprise a P-type transistor, are conducted by an over-driven signal.

10. The ferroelectric memory according to claim 5, wherein the sense amplifier is a latch sense amplifier.

11. A ferroelectric memory comprising:

a memory unit comprising:

a positive bit line and a negative bit line which are parallel to each other and are coupled to the sense amplifier;

a word line which is virtually perpendicular to the positive and the negative bit lines;

a positive memory cell which is coupled to the word line and the positive bit line and will be connected to the positive bit line when the word line is enabled;

a negative memory cell which is coupled to the word line and the negative bit line and will be connected to the negative bit line when the word line is enabled; and

a plate line which is coupled to the positive and the negative memory units; and

a sense amplifier, comprising:

a first phase inverter whose outlet and input ends are coupled to the positive and the negative bit lines respectively, outputting the voltage in the negative bit line after having inverted the phase of the voltage in the negative bit line, comprising a first P-type transistor and a first N-type transistor, wherein the gate electrodes of the first P-type transistor and the first N-type transistor are coupled to the negative bit line while the drain of the first P-type transistor and the source electrode of the first N-type transistor are coupled to the outlet end of the first phase inverter;

a second phase inverter whose input and outlet ends are coupled to the positive and the negative bit line respectively, outputting the voltage in the positive bit line after having inverted the phase of the voltage in the positive bit line, comprising a second P-type transistor and a second N-type transistor, wherein the gate electrodes of the second P-type transistor and the second N-type transistor are coupled to the positive bit line while the drain of the second P-type transistor and the source electrode of the second N-type transistor are coupled to the outlet end of the second phase inverter;

a P-switch with one end coupled to the source electrodes of the first and the second P-type transistors and the other end coupled to a power

source; and

an N-switch with one end coupled to the drains of the first and the second N-type transistors and the other end grounded.

12. The ferroelectric memory according to claim 11, wherein the ferroelectric memory is applied in a plate-line driven access method which comprises the steps of:

enabling the word line;

enabling the plate line to generate a voltage difference between the positive bit line and the negative bit line;

enabling the N-switch to enlarge the voltage difference;

enabling the P-switch to have the sense amplifier be enabled to further enlarge the voltage difference by raising the higher voltage among the voltage in the positive bit line and the voltage in the negative bit line to high level but reducing the lower voltage to low level; and

sensing the voltage difference between the positive bit line and the negative bit line and outputting the content stored at the ferroelectric memory accordingly.

13. The ferroelectric memory according to claim 11, wherein the ferroelectric memory is applied in a bit-line driven access method which comprises the steps of:

pre-charging the positive and the negative bit lines;

enabling the word line to generate a voltage difference between the positive bit line and the negative bit line;

enabling the P-switch to enlarge the voltage difference;

enabling the N-switch to have the sense amplifier be enabled to further enlarge the voltage difference; and

sensing the voltage difference between the positive bit line and the negative bit line and outputting the content stored at the ferroelectric memory accordingly.

14. The ferroelectric memory according to claim 11, wherein switch P is a P-type transistor.

15. The ferroelectric memory according to claim 11, wherein switch N is an N-type transistor.

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